Amendments to the Claims

Please amend the claims as follows:

1. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising a plurality of lower metal layers and an upper metal layer; with at least one of the lower metal layers of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

2. (original) The bond pad structure of Claim 1, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

3. (canceled)

4. (currently amended) The bond pad structure of Claim ~~3~~ 1, wherein at least two lower metal layers of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

5. (original) The bond pad structure of Claim 1, further comprising a conductive material interconnecting the first bond pad to the second bond pad.

6. (original) The bond pad structure of Claim 5, wherein the conductive material comprises a solder material.

7. (original) The bond pad structure of Claim 5, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

8. (original) The bond pad structure of Claim 5, further comprising a bonding wire connected to the conductive material.

9. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising a plurality of lower metal layers and an upper metal layer; with a at least one of the lower metal layers of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; wherein the extension of the at least one lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

10. (original) The bond pad structure of Claim 9, further comprising a conductive material interconnecting and overlying at least a portion of the first and second bond pads.

11. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

12. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

13. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad interconnected to a second bond pad by a conductive material; each of the bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

14. (original) The bond pad structure of Claim 13, wherein the conductive material overlies a portion of each of the bond pads.

15. (original) The bond pad structure of Claim 13, wherein the conductive material comprises a solder material.

16. (original) The bond pad structure of Claim 13, further comprising a bonding wire connected to the conductive material.

17. (original) The bond pad structure of Claim 13, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

18. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first bond pad and a second bond pad positioned within a single passivation opening; the first and second bond pads interconnected by a conductive material overlying at least a portion of each of the bond pads; and each of the bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

19. (original) The bond pad structure of Claim 18, further comprising a passivation layer overlying a portion of each of the bond pads, the opening being formed through the passivation layer to expose the bond pads.

20. (original) The bond pad structure of Claim 18, wherein the conductive material comprises solder.

21. (original) The bond pad structure of Claim 18, further comprising a bonding wire connected to the conductive material.

22. (currently amended) A bond pad structure in a semiconductor ~~device~~ die, comprising:

a first metal layer deposited onto a substrate and patterned to form first and second lower metal layer portions having a space thereinbetween;

a dielectric layer deposited over the first and second lower metal layer portions and the substrate within the space, and etched to form openings to each of the first and second lower metal layer portions;

a second metal layer deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first and second upper metal layer portions overlying and in conductive contact with the first and second lower metal layer portions; the first upper and lower metal layer portions forming a first bond pad, and the second upper and lower metal layer portions forming a second bond pad; and

a conductive material comprising a solder material situated on and interconnecting the first bond pad ~~to~~ and the second bond pad;

wherein a lower metal layer portion of one of the bond pads extends beneath the upper metal layer portion of the other of the bond pads.

23. (original) The bond pad structure of Claim 22, further comprising a passivation layer formed over the bond pads and etched to form an opening therethrough to expose the first and second bond pads.

24-25. (canceled)

26. (previously presented) The bond pad structure of Claim 22, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

27. (previously presented) The bond pad structure of Claim 22, further comprising a bonding wire connected to the conductive material.

28. (currently amended) A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and

at least one of the bond pads functions to supply data, retrieve data, test a device, or supply various voltage levels; wherein the first bond pad is functional only in an operational

mode, and the second bond pad is functional in a test mode and in an operation mode ~~upon discontinuing the test mode and being interconnected to the first bond pad~~.

29. (canceled)

30. (currently amended) The bond pad structure of Claim ~~29~~ 28, wherein the lower metal layer of the first bond pad extends beneath the upper metal layer of the second bond pad.

31. (currently amended) The bond pad structure of Claim ~~29~~ 28, wherein the lower metal layer of the second bond pad extends beneath the upper metal layer of the first bond pad.

32. (currently amended) A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; and

the first bond pad functional to receive and respond to a test mode signal by entering a test mode and the second bond pad functional only in an operational mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to a receive and respond to an operational mode signals by entering an operational mode.

33. (original) The bond pad structure of Claim 32, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

34. (original) The bond pad structure of Claim 32, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

35-49. (canceled)

50. (previously presented) An integrated circuit die, comprising:

a first bond pad and a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

51. (original) The integrated circuit die of Claim 50, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

52. (original) The integrated circuit die of Claim 50, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

53. (original) The integrated circuit die of Claim 50, further comprising a conductive material interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

54. (original) The integrated circuit die of Claim 53, wherein the conductive material comprises solder.

55. (original) The integrated circuit die of Claim 53, further comprising a bonding wire connected to at least one of the bond pads.

56. (canceled)

57. (original) The integrated circuit die of Claim 50, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

58. (previously presented) An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening;

each of the first and second bond pads comprising at least two lower metal layers and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

59. (original) The integrated circuit die of Claim 58, wherein the first and second bond pads are interconnected by a conductive material interconnecting overlying and in conductive contact with at least a portion of each of the bond pads.

60. (previously presented) An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least two lower metal layers and an upper metal layer; and the lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

61. (previously presented) An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least two lower metal layers and an upper metal layer; with the lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

62. (previously presented) An integrated circuit die, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least two lower metal layer and an upper metal layer; the lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages.

63. (original) The integrated circuit die of Claim 62, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

64. (currently amended) The integrated circuit die of Claim 62, wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode, and the second bond pad is functional solely in an operational mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode.

65. (original) The integrated circuit die of Claim 64, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

66-68. (canceled)

69. (currently amended) A semiconductor die comprising a bond pad structure disposed on a substrate and comprising multiple bond pads, each bond pad comprising overlying upper and lower metal layers, and each bond pad comprising two or more lower metal layers, and the upper metal layer of one of the bond pads overlapping the lower metal layer of another of the bond pads.

70. (currently amended) A semiconductor die comprising a bond pad structure disposed on a substrate and comprising two or more bond pads, each bond pad comprising an overlying upper and two or more lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

71. (currently amended) A bond pad structure disposed on a substrate and comprising:

a lower metal layer disposed on the substrate and comprising first and second portions separated by a space therebetween;

a dielectric layer overlying the lower metal layer and the substrate within the space; one or more openings extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer disposed over the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad; and

a conductive solder material situated on and interconnecting the first bond pad ~~to~~ and the second bond pad.

72. (previously presented) An integrated circuit supported by a substrate and comprising: a bond pad structure, the bond pad structure comprising two or more bond pads, each bond pad comprising an overlying upper and two or more lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

73. (previously presented) An integrated circuit supported by a substrate and comprising: a first bond pad and a second bond pad; each of the bond pads comprising two or more lower metal layers and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond at least one of the two or more lower metal layers of the one bond pad and over at least one of the two or more lower metal layers of the other of the bond pads.

74. (currently amended) An integrated circuit supported by a substrate and comprising a bond pad structure, the bond pad structure comprising:

a lower metal layer comprising first and second portions with a space therebetween;

a dielectric layer overlying the lower metal layer and within the space; at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper

metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad;

wherein the first bond pad is functional solely in an operational mode, and the second bond pad is functional in a test mode, and in an operation mode upon discontinuing the test mode and being interconnected to the first bond pad.

75. (currently amended) A semiconductor ~~device~~ die, comprising:

a substrate; and

a bond pad structure disposed on the substrate, the bond pad structure comprising multiple bond pads, each bond pad comprising an overlying upper and two or more lower metal layers, and the upper metal layer of one of the bond pads overlaps at least one of the lower metal layers of another of the bond pads.

76. (currently amended) A semiconductor wafer, comprising:

a substrate and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad and a second bond pad; each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond the lower metal layer of the one bond pad and over the lower metal layer of the other of the bond pads;

wherein the first bond pad is functional only in an operational mode, and the second bond pad is functional in a test mode and in an operation mode ~~upon discontinuing the test mode and being interconnected to the first bond pad~~.

77. (currently amended) A semiconductor wafer, comprising:

a semiconductor die comprising a substrate and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad and a second bond pad interconnected by a conductive solder material; each bond pad comprising an upper metal layer overlying two or more lower metal layers, the upper metal layer of one of the bond pads overlapping at least one of the lower metal layers of another of the bond pads.

78. (currently amended) A semiconductor wafer, comprising:

a substrate and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad and a second bond pad interconnected by a conductive solder material; each bond pad comprising an upper metal layer overlying two or more lower metal layers, the upper metal layer of one of the bond pads overlapping at least one of the lower metal layers of another of the bond pads;

wherein the first bond pad is functional solely in an operational mode, and the second bond pad is functional in a test mode and in an operation mode ~~upon discontinuing the test mode and being interconnected to the first bond pad~~.